Catalyst N3: A 128-Core Hybrid Neuromorphic Processor with Hardware Virtualisation, Per-Tile Learning, and Silicon Metaplasticity

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Abstract

We present **Catalyst N3**, the third generation of the Catalyst neuromorphic processor architecture. Where N1 matched Intel Loihi 1 and N2 achieved full Loihi 2 feature parity, N3 moves beyond parity to introduce capabilities absent from all current neuromorphic hardware. The architecture comprises 128 cores organised into 16 tiles of 8 cores each, supporting 524K physical neurons at 24-bit precision or 4.2 million virtual neurons through hardware time-division multiplexing. A four-thread parallel microcode engine with 80 registers enables eight hardwired neuron models—including INT8 multiply-accumulate for conventional neural networks—plus a user-defined custom model via a 13-opcode instruction set. Four configurable synapse formats (72-bit full, 49-bit inference, 20-bit compact, and 35-bit low-rank FACTOR) support variable-precision weights from 1 to 16 bits. Sixteen per-tile learning accelerators, each with a 28-opcode instruction set and four-stage pipeline, eliminate the cross-chip learning bottleneck present in prior architectures. Hardware metaplasticity via 3-bit per-synapse consolidation and homeostatic plasticity via EWMA firing-rate tracking provide silicon-native network stabilisation without software intervention. A three-level asynchronous-synchronous hybrid network-on-chip with adaptive routing, express links, and spike compression achieves near-zero idle power. The accompanying `neurocore` SDK (v3.7.0) provides 88 modules, 3,091 tests, and three interchangeable backends (CPU, GPU, FPGA), enabling a seamless path from research to hardware deployment. We validate an 8-core tile on an AWS F2 Xilinx VU47P FPGA at 62.5 MHz, achieving 19/19 hardware test pass rate and 14,512 timesteps per second. Benchmark evaluation on the Spiking Speech Commands dataset yields **76.4%** test accuracy—a new state of the art, exceeding Intel Loihi 2 (69.8%) by 6.6 percentage points and the previous best software result (74.2%) by 2.2 points. On Spiking Heidelberg Digits, N3 achieves **91.0%** test accuracy, exceeding both our N2 baseline (90.7%) and Intel Loihi 2 (90.9%). ASIC characterisation via Yosys and OpenLane (SKY130 130 nm) yields over 1.5 million estimated gates per core, with block-level place-and-route confirming the router at 89,812 cells and a clean host interface at 3,807 cells; geometric scaling projects approximately 58 mm^2 per tile at 28 nm. The architecture is specified in a 78-page technical specification (v3.0, 68 features), implemented in 46 synthesisable Verilog files totalling approximately 17,700 lines with 897 assertions, and validated across 1,011 simulation tests in 57 testbenches. Catalyst N3 is, to our knowledge, the first neuromorphic architecture to unify spiking and conventional neural network execution, hardware virtualisation, and silicon-native metaplasticity in a single chip.

1 Introduction

Biological neural systems process information with extraordinary energy efficiency. A human cortex, operating on roughly 20 watts, sustains real-time sensory processing, motor control, memory consolidation, and abstract reasoning across 10^{11} neurons and 10^{14} synapses [10]. Neuromorphic processors aim to replicate this efficiency by co-locating computation and memory, communicating via sparse binary spikes, and supporting local synaptic plasticity. The past decade has produced several landmark chips: Intel's Loihi 1 and Loihi 2 [3, 4], IBM's TrueNorth [5], SpiNNaker 1 and 2 [6, 7], and BrainScaleS-2 [8].

Yet a gap remains. No current neuromorphic processor unifies spiking and conventional neural network execution on the same substrate. None provides hardware virtualisation that time-multiplexes physical cores across hundreds of virtual networks. None embeds metaplastic consolidation—the biological mechanism by which frequently reinforced synapses become resistant to overwriting—directly in silicon. And none distributes learning accelerators per tile, forcing all plasticity computation through a single global pipeline that bottlenecks at scale.

This paper presents Catalyst N3, which addresses each of these gaps. Building on the N1 foundation of Loihi 1 parity [1] and the N2 achievement of full Loihi 2 feature parity [2], N3 introduces 34 new architectural features that collectively represent a generational leap in neuromorphic hardware capability. The full architecture is specified in a 78-page technical specification (v3.0), implemented in 46 synthesisable Verilog files totalling approximately 17,700 lines of RTL with 897 assertions, and supported by the `neurocore` SDK (v3.7.0) with 88 modules, 3,091 tests, and three interchangeable backends spanning CPU simulation, GPU acceleration, and FPGA

deployment. ASIC characterisation via Yosys 0.34 and OpenLane 2 (SKY130 130 nm) confirms full synthesisability, with the router completing place-and-route at 89,812 cells and geometric scaling projecting approximately 58 mm^2 per tile at 28 nm.

Design philosophy. Three principles guided the N3 design:

1. **Hybrid computation.** Spiking neural networks excel at temporal and event-driven processing but struggle with tasks where conventional deep learning dominates. Rather than choosing one paradigm, N3 provides both: an INT8 multiply-accumulate mode coexists with eight spiking neuron models on every core. A single chip can run convolutional image classification on one tile and spike-timing-dependent plasticity on the next.
2. **Scalable autonomy.** Prior neuromorphic architectures centralise learning computation and network management. This creates bottlenecks: a single learning engine must service all 128 cores, and context switching between virtual networks requires host intervention. N3 decentralises both. Each tile has its own learning accelerator with a 28-opcode instruction set, and a hardware operating system (NeurOS) manages virtual network scheduling, DMA, and context switching without host involvement.
3. **Silicon-native plasticity.** Biological synapses do not merely strengthen and weaken. They consolidate [15], homeostatically regulate [16], fatigue under sustained activation, and respond to neuromodulatory signals [17]. Prior neuromorphic chips implement basic STDP but leave consolidation, homeostasis, and fatigue to software. N3 implements all three in hardware: 3-bit metaplastic consolidation per synapse, EWMA firing-rate tracking with threshold scaling per neuron group, and 4-bit synaptic fatigue per synapse. Networks running on N3 stabilise themselves.

Contributions. The specific contributions of this work are:

- A 128-core neuromorphic processor organised into 16 tiles, with a four-level memory hierarchy (96 KB L1 per core, 1 MB shared L2 per tile, LPDDR5X/HBM L3, and CXL L4) supporting 524K physical neurons or 4.2M virtual neurons through hardware time-division multiplexing.
- A four-thread parallel microcode engine with 80 registers enabling eight hardwired neuron models plus user-defined custom dynamics via a 13-opcode ISA, and parameter groups that quadruple per-core neuron density from 1,024 to 4,096 at 24-bit precision.
- Four configurable synapse formats including a 35-bit FACTOR low-rank representation achieving 2–8$\times$ memory compression, with variable-precision weights from 1 to 16 bits and 4-bit per-synapse fatigue tracking.
- Sixteen per-tile learning accelerators with a 28-opcode ISA (v3.5), 16-channel neuromodulation, hardware metaplasticity (3-bit consolidation), homeostatic plasticity (EWMA rate tracking), and lazy eligibility decay via pre-computed lookup tables.
- A three-level asynchronous-synchronous hybrid network-on-chip with minimal adaptive routing, 8 express links per tile, 256 multicast groups per tile, and DELTA/BURST/ADAPTIVE spike compression achieving 2–8$\times$ bandwidth reduction.
- Per-tile power gating (7-state FSM with wake-on-spike), per-pipeline-stage clock gating, ECC scrubbing, and a deterministic execution mode with LFSR seeding and GALS bypass for fully reproducible computation.
- The `neurocore` SDK (v3.7.0) with 88 modules, 3,091 tests, and three backends (CPU cycle-accurate simulator, GPU PyTorch simulator, and FPGA PCIe backend), providing a complete toolchain from network description through compilation to hardware deployment.
- FPGA validation of an 8-core tile on AWS F2 (Xilinx VU47P) at 62.5 MHz with 19/19 hardware tests passing and 14,512 timesteps per second throughput, alongside 1,011 simulation tests across 57 testbenches.
- Benchmark evaluation establishing a new state of the art on Spiking Speech Commands (76.4%, exceeding Loihi 2 by 6.6 points) and Spiking Heidelberg Digits (91.0%, exceeding Loihi 2's 90.9%), with N2 generational baselines on N-MNIST (99.2%) and Google Speech Commands (88.0%) demonstrating progressive architectural improvement.

Paper organisation. Section 2 recaps the N2 baseline. Section 3 presents the N3 architecture overview. Section 4 details the programmable neuron engine. Section 5 covers synapse architecture. Section 6 describes the learning and plasticity system. Section 7 presents the network-on-chip. Section 8 covers efficiency and virtualisation features. Section 9 addresses reliability and determinism. Section 10 presents the SDK and software stack. Section 11 presents FPGA implementation, the 27-build validation narrative, and ASIC exploration results. Section 12 evaluates benchmark performance across four tasks. Section 13 surveys related work. Section 14 discusses limitations honestly, and Section 15 concludes.

2 N2 Baseline

For readers unfamiliar with the preceding papers [1, 2], we summarise the N2 architecture that serves as N3's foundation.

Catalyst N2 achieved full feature parity with Intel's Loihi 2. The architecture comprises 128 cores, each containing 1,024 CUBA LIF neurons with 24-bit state precision, configurable synaptic connectivity in three formats (sparse, dense, and population), and a programmable neuron microcode engine supporting five neuron models: CUBA, Izhikevich [11], adaptive LIF [12], sigma-delta [13], and resonate-and-fire [14]. Variable-precision weight packing (1–16 bit) and four graded spike payload formats (binary through 24-bit) provide flexible data representation. A 16-opcode learning engine with per-synapse-group plasticity control, five independent trace time constants, persistent reward traces, and homeostatic threshold plasticity rounds out the plasticity support.

The accompanying SDK grew from 14 modules and 168 tests (N1) to 88 modules and 3,091 tests across three backends. A systematic feature parity assessment identified 155 Loihi 2 features, of which 152 were fully implemented; the three remaining features require physical multi-chip links. FPGA validation on AWS F2 achieved 28/28 test pass rate at 62.5 MHz.

N2 was a necessary achievement: it proved that an independently developed architecture could match Intel's commercial processor feature-for-feature. But matching is not leading. N2's neuron pipeline processes one model at a time. It lacks conventional neural network support. Context switching between virtual networks requires host orchestration. And all learning computation flows through a single global pipeline. N3 addresses each of these limitations.

3 Architecture Overview

3.1 System Topology

N3 organises 128 neuromorphic cores into 16 tiles of 8 cores each (Figure 1). Each tile constitutes an autonomous processing unit: 8 cores share a 1 MB L2 SRAM cache, a dedicated learning accelerator, a routing tile with spike compression, and an independent power domain with per-tile gating. The tile is the unit of power management, learning computation, and virtual network scheduling.

Tiles connect through a hierarchical fat-tree network-on-chip with 8 express bypass links per tile. Off-chip connectivity is provided by CXL 2.0 and 8 Address-Event Representation (AER) links for multi-chip scaling. A host interface via AXI4-Lite provides configuration, monitoring, and stimulus injection. A global RISC-V management core handles boot sequence, interrupt dispatch, performance counter collection, and inter-tile barrier synchronisation.

3.2 Memory Hierarchy

N3 introduces a four-level memory hierarchy—the deepest of any neuromorphic architecture:

1. **L1 (96 KB per core):** Neuron state, synapse weights, delay queues, and learning traces. Organised as approximately 51 independent SRAMs per core, matching the N1/N2 layout but with configurable precision allocation: 4,096 neurons at 24-bit, 8,192 at 16-bit, or 12,288 at 8-bit. Each SRAM is protected by SEC-DED ECC with background scrubbing (Section 9).
2. **L2 (1 MB per tile, shared):** Spillover synapses, parameter group tables, and frequently accessed weight matrices shared across cores within a tile. Accessed via a per-tile cache controller with tag-based lookup. The cache controller supports four eviction policies: LRU (default), FIFO, random, and fixed. A 64-entry DMA descriptor table manages scatter-gather transfers between L2 and L3.
3. **L3 (LPDDR5X or HBM):** Off-tile storage for large synapse tables, virtual network contexts, and checkpoint data. DMA scatter-gather with 64-entry descriptor tables and dirty tracking enables efficient context migration. Supports 500M+ addressable synapses. A spike prefetcher with spatial and burst detection pre-loads synapse groups into L2 before they are needed, hiding L3 access latency for regular spike patterns.
4. **L4 (CXL 2.0):** Coherent memory access for multi-chip configurations and host-side data sharing. Provides load/store semantics to remote chip memory without explicit message passing. The CXL interface supports both CXL.mem (host-managed device memory) and CXL.cache (device-coherent host memory), enabling the host to read neuron state without stalling the neuromorphic pipeline.

The four-level hierarchy addresses a fundamental tension in neuromorphic design: biological networks have far more synapses than can fit in on-chip SRAM, but off-chip access destroys the energy efficiency that motivates neuromorphic computation. N3 resolves this with prefetching (a spike prefetcher with spatial and burst detection) and context-aware caching (recently accessed synapse groups remain in L2 across timesteps).

3.3 Per-Core Capacity

The introduction of parameter groups—32 groups of shared neuron parameters per core—transforms N3's per-core capacity. In N1 and N2, each neuron stored its own 38 parameters individually, consuming approximately 46 KB of L1 per 1,024 neurons. In N3, neurons reference a 5-bit group selector, and only per-neuron state (membrane potential, adaptation variable, traces) is stored individually. The full parameter groups mechanism is detailed in Section 4.3; the net effect is a reduction of per-neuron overhead from approximately 46 bytes to approximately 12 bytes, enabling **4,096 neurons per core** in the same 96 KB L1—a 4× improvement.

At chip scale, 128 cores × 4,096 neurons yields **524,288 physical neurons** at 24-bit precision. At 16-bit precision, neuron density doubles to 8,192 per core (1,048,576 total). At 8-bit precision (useful for inference-only networks), density triples to 12,288 per core (1,572,864 total). With time-division multiplexing (Section 8), effective capacity reaches **4.2 million virtual neurons** (128 cores × 4,096 neurons × 8 TDM slots at full depth, or 32 slots at 1,024 neurons).

3.4 Per-Core SRAM Budget

Table 1 provides a detailed breakdown of the 96 KB L1 allocation per core. The budget is designed for the full-featured configuration (4,096 neurons, 24-bit state, Full synapse format with learning). Networks that use inference-only synapse formats or reduced precision can reallocate unused SRAM banks to increase neuron or synapse capacity.

The neuron state allocation (40 KB) stores four 24-bit values per neuron—membrane potential v, dendritic current u, refractory counter, and auxiliary state—across 4,096 neurons. The

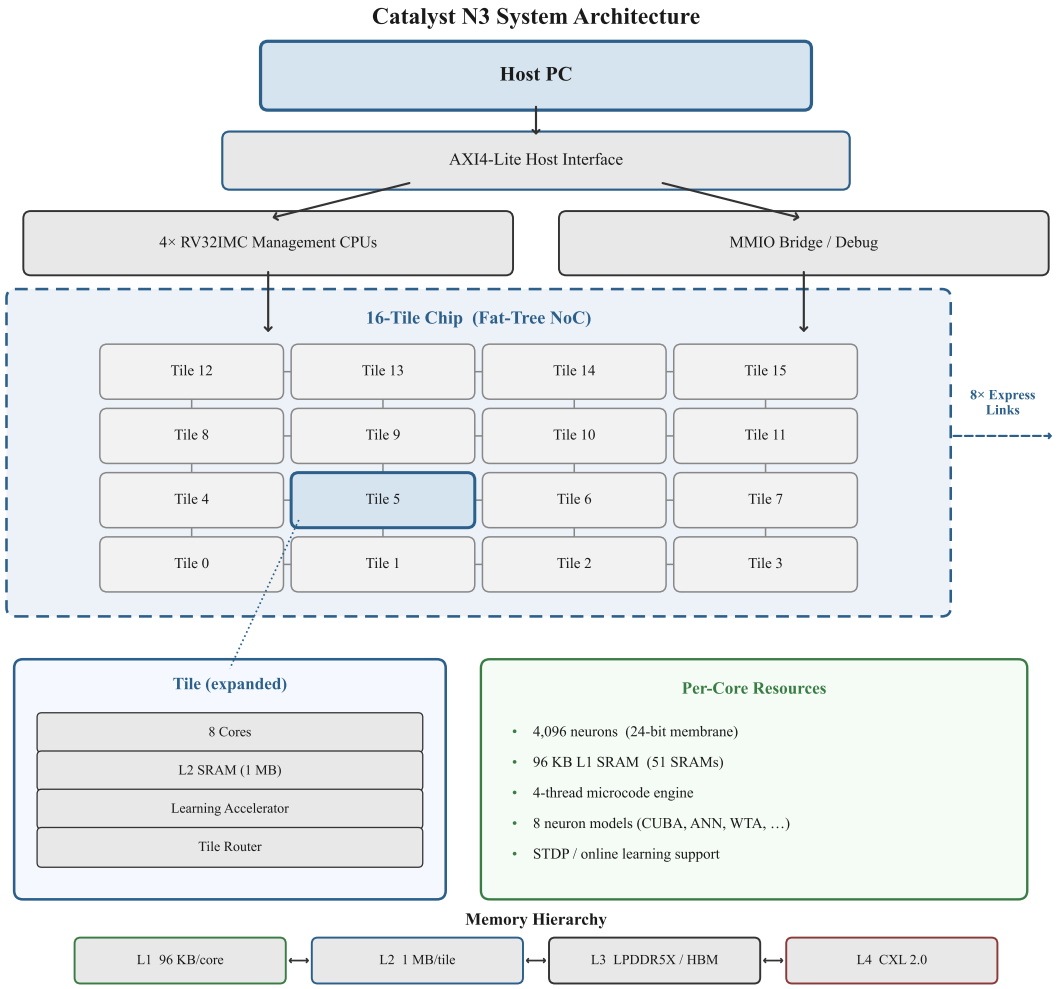

Figure 1: Catalyst N3 system architecture. 128 neuromorphic cores are organised into 16 tiles of 8 cores each. Each tile contains a shared L2 SRAM cache, a dedicated learning accelerator, a routing tile with spike compression, and an independent power domain. Tiles connect via a hierarchical fat-tree NoC with express bypass links. Off-chip interfaces include CXL 2.0 coherent memory, 8 AER multi-chip links, and an AXI4-Lite host interface.

Table 1: Per-core L1 SRAM budget breakdown (96 KB total).

Component	**Size**
Neuron state (v, u, refrac, aux)	40 KB
Pre/post synaptic traces	20 KB
Parameter group selectors (5-bit × 4096)	3 KB
Parameter group tables (32 × 38 params)	2 KB
Synapse index (fanin pointers)	8 KB
Hot synapse cache	12 KB
Microcode store (4 threads × 32 instr.)	1 KB
Delay queue (8-bit delay, 256-deep)	4 KB
Spike buffers (in/out FIFOs)	4 KB
Configuration registers + status	2 KB
Total	**∼96 KB**

trace allocation (20 KB) stores pre-synaptic trace x_1 and post-synaptic traces y_1, y_2 at configurable precision (8 or 16 bits per trace). The hot synapse cache (12 KB) provides a small fast-access buffer for the most recently accessed synapse groups, reducing L2 fetch latency for recurrent connections where the same synapses are accessed every timestep. The microcode store (1 KB) holds the four-thread program (32 instructions per thread, 8 bytes per instruction), and the delay queue (4 KB) implements axonal delay with 8-bit delay values supporting up to 255 timestep delays across 256 queue entries per core.

4 Programmable Neuron Engine

4.1 Four-Thread Parallel Microcode

N2's neuron microcode engine processes one neuron at a time through a single-threaded pipeline. N3 extends this to **four parallel microcode threads** sharing a single ALU via round-

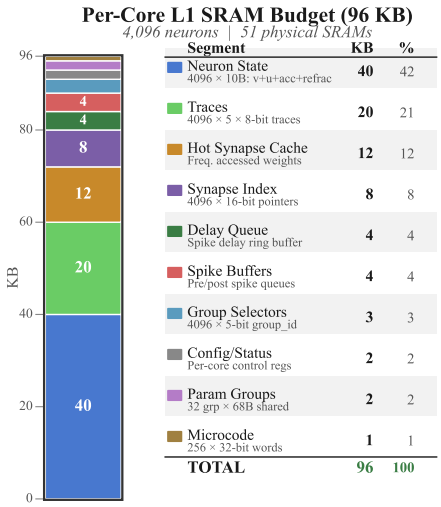

Figure 2: Per-core L1 SRAM budget visualisation. Neuron state and traces dominate the allocation, reflecting the architecture's focus on rich per-neuron dynamics and on-chip learning. The hot synapse cache and synapse index together provide high-bandwidth local weight access.

robin scheduling (Figure 3). Each thread maintains its own program counter and 20-register slice of the 80-register file, enabling four neurons to be in different stages of computation simultaneously. The shared ALU amortises hardware cost: a single multiply-shift unit serves all four threads, with each thread receiving one ALU slot every four cycles.

The register file is organised as follows: registers R0–R7 are neuron state (membrane potential, threshold, adaptation, refractory counter, accumulator, gating signal, trace values, auxiliary), R8–R15 are synapse/learning scratch space, and R16–R19 are control registers (program counter, neuron ID, parameter group index, status flags). All registers are 24-bit to match the neuron state precision.

The four-thread design delivers a 3.2× throughput improvement over the single-threaded N2 pipeline (not 4×, due to occasional ALU bank conflicts when two threads require the multiply unit simultaneously). An **activity bitmap** (one bit per neuron, 512 bytes per core for 4,096 neurons) tracks which neurons received synaptic input during the current timestep. Neurons with no input and membrane potential below the approximate-computing threshold (Section 8) are skipped entirely, yielding further speedup proportional to network sparsity.

4.2 Neuron Models

N3 supports eight hardwired neuron models selectable per parameter group, plus a user-defined custom model:

Table 2: N3 neuron models and their primary characteristics.

#	Model	Key Feature
0	CUBA/LIF	Loihi-compatible, dendritic compartments
1	ANN	INT8 MAC for conventional NNs
2	WTA	Winner-take-all, configurable k
3	ALIF	Adaptive threshold, exponential decay
4	Sigma-Delta	Change-detection encoding
5	Gated	Multiplicative accumulator gating
6	Graded	Continuous 8/16-bit spike payload
7	Custom	13-opcode ISA, 8 registers

CUBA/LIF (Model 0). The baseline model preserves full backward compatibility with N1 and N2:

$$u[t] = u[t-1] - \mathrm{RAZ}(\texttt{decay\_u} \cdot u) + I_{\text{syn}} \quad (1)$$

$$v[t] = v[t-1] - \mathrm{RAZ}(\texttt{decay\_v} \cdot v) + u + \texttt{bias} \quad (2)$$

where RAZ denotes round-away-from-zero fixed-point arithmetic matching Loihi's hardware rounding. A spike is emitted when $v[t] \geq \theta$ and the refractory counter is zero. The refractory counter is loaded with `refrac_delay` upon spike emission and decrements each timestep until zero. Dendritic compartments share the same equations but accumulate into separate dendritic state variables before summing into the somatic accumulator.

ANN Mode (Model 1). This is a qualitative departure from spiking computation. In ANN mode, each core operates as a conventional INT8 matrix-vector multiply-accumulate unit:

$$\text{acc} = \sum_i w_i \cdot x_i, \qquad \text{output} = \text{clamp}(\text{acc} \gg \text{shift},\ 0,\ 255) \quad (3)$$

where w_i and x_i are 8-bit signed integers, the accumulator `acc` is 32-bit, and `shift` is a per-group configurable right-shift (0–15) that controls the output scale. The output is emitted as a graded spike (8-bit payload) if it exceeds a configurable threshold θ_{ann}. The INT8 MAC pipeline processes one synapse per cycle per thread; with four threads active, peak throughput is 4 MACs/cycle at 62.5 MHz (FPGA) or the target ASIC frequency. To our knowledge, N3 is the first neuromorphic processor to provide native ANN execution on the same silicon as SNN processing. This enables hybrid architectures where, for example, a convolutional feature extractor (ANN mode) feeds into a temporal classifier (SNN mode) without off-chip data transfer.

Winner-Take-All (Model 2). The WTA model implements a two-pass lateral inhibition algorithm. In the first pass, all neurons in the group compute their membrane potential normally using Equations (1)–(2). The neuron engine then identifies the top-k neurons by membrane potential:

$$S_k = \text{top-}k(\{v_i[t]\}_{i \in \text{group}}), \qquad s_i[t] = \begin{cases} 1 & \text{if } v_i \in S_k \\ 0 & \text{otherwise} \end{cases} \quad (4)$$

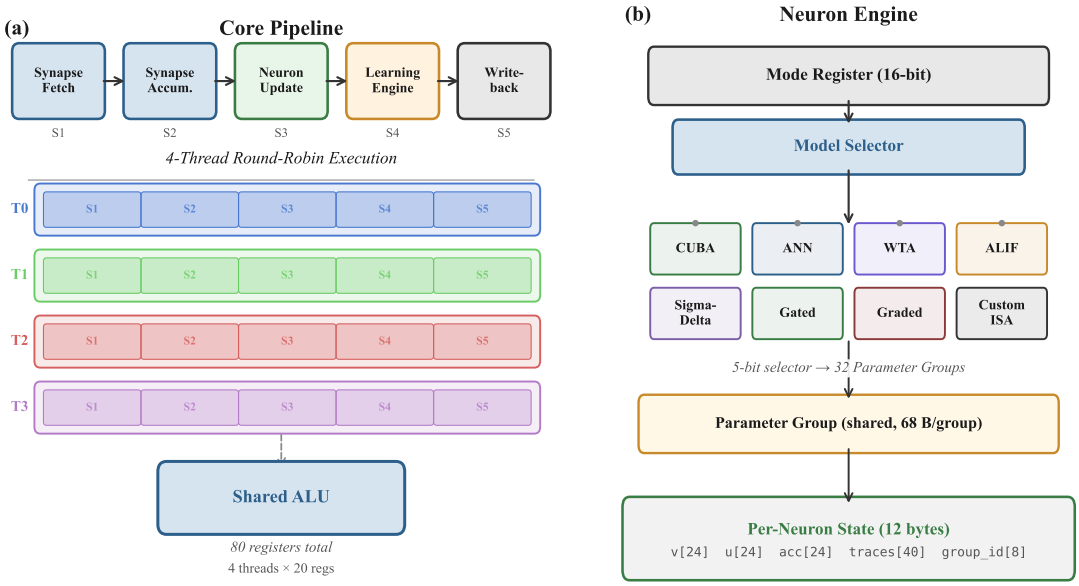

Figure 2. Core pipeline and neuron engine.

Figure 3: Core pipeline and neuron engine architecture. Four microcode threads share a single ALU via round-robin arbitration. Each thread maintains 20 registers (R0–R19) and an independent program counter. The pipeline stages—synapse delivery, neuron update, spike generation, and writeback—operate concurrently across threads, with per-stage clock gating (ICG cells) to eliminate dynamic power for idle stages. The activity bitmap (one bit per neuron) allows the pipeline to skip neurons that received no input and are below the approximate-computing threshold.

where k is configurable per parameter group (1–8). Neurons outside S_k have their membrane potential reset. The two-pass approach avoids the need for explicit lateral inhibitory synapses, saving synapse memory and simplifying network topology for classification tasks.

Adaptive LIF (Model 3). The ALIF model extends the LIF neuron with a spike-frequency adaptation mechanism [12]:

$$\theta_{\text{adapt}}[t] = \theta_{\text{adapt}}[t-1] - \text{RAZ}(\texttt{decay\_}\theta \cdot \theta_{\text{adapt}}) + s[t] \cdot \Delta\theta \tag{5}$$

$$\theta_{\text{eff}}[t] = \theta_{\text{base}} + \theta_{\text{adapt}}[t] \tag{6}$$

where $s[t] \in \{0, 1\}$ is the spike indicator and $\Delta\theta$ is the per-spike increment. The adaptive threshold θ_{eff} rises after each spike and decays exponentially toward θ_{base}, producing intrinsic spike-frequency adaptation that is critical for temporal pattern recognition tasks such as speech classification.

Sigma-Delta (Model 4). The sigma-delta neuron implements change-detection encoding, converting continuous input signals into sparse spike trains that represent *changes* rather than absolute values:

$$\delta[t] = x[t] - \hat{x}[t] \tag{7}$$

$$s[t] = \begin{cases} +1 & \text{if } \delta[t] > \theta_{\text{sd}} \\ -1 & \text{if } \delta[t] < -\theta_{\text{sd}} \\ 0 & \text{otherwise} \end{cases} \tag{8}$$

$$\hat{x}[t] = \hat{x}[t-1] + s[t] \cdot \theta_{\text{sd}} \tag{9}$$

where $x[t]$ is the input, $\hat{x}[t]$ is the reconstructed estimate, and θ_{sd} is the change-detection threshold. The spike carries a signed 1-bit payload indicating increase or decrease. This encoding achieves high compression for slowly varying signals: a constant input produces zero spikes, regardless of its magnitude.

Gated (Model 5). The gated neuron model provides multiplicative modulation of the accumulator, inspired by gating mechanisms in LSTMs and attention:

$$\text{acc\_gated}[t] = \text{acc}[t] \cdot g[t] \tag{10}$$

where $g[t]$ is a modulatory input received on a dedicated gating dendritic compartment. The gating signal $g[t]$ is an 8-bit unsigned value (0–255, interpreted as a fraction 0.0–1.0 with 8-bit resolution). When $g = 0$, the accumulator is fully suppressed; when $g = 255$, it passes unattenuated. This enables

attention-like selective amplification of specific input pathways without requiring explicit multiplicative synapses.

Graded (Model 6). The graded neuron emits a continuous-valued output rather than a binary spike:

$$\text{output}[t] = \text{clamp}\big(v[t],\ 0,\ 2^P - 1\big) \tag{11}$$

where P is the payload precision (8 or 16 bits, configurable per parameter group). The output is transmitted as a graded spike with a P-bit payload. Unlike the ANN model (which skips the spiking dynamics entirely), the graded model computes membrane potential using the standard LIF equations and then emits the clamped value—combining spiking dynamics with continuous output for applications such as population coding and probabilistic inference.

Custom Model (Model 7). For researchers requiring neuron dynamics not captured by the seven hardwired models, the custom model provides a 13-opcode instruction set architecture with 8 dedicated registers (separate from the thread's main register file). The user writes a microcode program of up to 32 instructions using the opcodes listed in Table 3.

Table 3: Custom neuron model ISA (13 opcodes).

Opcode	Syntax	Description
ADD	Rd, Rs1, Rs2	Rd ← Rs1 + Rs2
SUB	Rd, Rs1, Rs2	Rd ← Rs1 − Rs2
MUL>>8	Rd, Rs1, Rs2	Rd ← (Rs1×Rs2) ≫ 8
SHR	Rd, Rs, imm	Rd ← Rs ≫ imm
SHL	Rd, Rs, imm	Rd ← Rs ≪ imm
CLAMP	Rd, Rs, lo, hi	Rd ← min(max(Rs, lo), hi)
LOAD_IMM	Rd, imm16	Rd ← imm16 (sign-extended)
LOAD_ACC	Rd	Rd ← accumulator
STORE_V	Rs	v ← Rs (write membrane)
CMP_GT	Rd, Rs1, Rs2	Rd ← (Rs1 > Rs2) ? 1 : 0
BRANCH	Rs, offset	If Rs ≠ 0, PC ← PC + offset
SPIKE	—	Emit spike, continue
HALT	—	End neuron update

The program executes each timestep, reading synaptic input from the accumulator via LOAD_ACC and writing the updated membrane potential via STORE_V. The SPIKE opcode emits a spike mid-program (for models that spike and then continue computing, such as burst models), while HALT terminates the update. As an example, a minimal Izhikevich neuron [11] can be implemented in 12 instructions using the custom ISA.

4.3 Parameter Groups

Each core maintains 32 parameter groups, where each group stores 38 neuron parameters (threshold, decay rates for u and v, refractory period, dendritic configuration, bias, trace enables, trace decay rates, noise amplitude, noise type, approximate-computing threshold, neuromodulation source selector, homeostatic target rate, and model-specific parameters) shared by all neurons assigned to that group. Each neuron stores only a 5-bit group selector alongside its per-neuron state.

The storage savings are quantified as follows. In N2, per-neuron storage is approximately 46 bytes (38 parameters at variable width, plus 6 bytes of state). In N3, per-neuron storage is:

$$\begin{aligned}\text{per-neuron} = &\underbrace{3}_{\text{v}} + \underbrace{3}_{\text{u}} + \underbrace{1}_{\text{refrac}} + \underbrace{1}_{\text{aux}} \\ &+ \underbrace{2}_{\text{traces}} + \underbrace{1}_{\text{flags}} + \underbrace{1}_{\text{grp sel}} = 12 \text{ bytes}\end{aligned} \tag{12}$$

The shared parameter group overhead is:

$$\text{groups total} = 32 \text{ groups} \times 38 \text{ params} \times \bar{w} \approx 2\,\text{KB} \tag{13}$$

where $\bar{w} \approx 1.7$ bytes is the average parameter width. This 2 KB overhead is amortised across all neurons in the core. At 4,096 neurons × 12 bytes = 48 KB for state, plus 2 KB for group tables, the neuron subsystem uses 50 KB of the 96 KB L1—leaving 46 KB for synapses, traces, queues, and microcode (Table 1).

The trade-off is that neurons within a group share parameters—acceptable for most practical networks, where neurons within a layer typically share the same configuration. For networks requiring per-neuron parameter variation, a single core can be configured with 32 groups of 128 neurons each, providing 32 distinct parameter sets.

5 Synapse Architecture

5.1 Configurable Synapse Formats

N3 introduces four synapse word formats, selectable per synapse group:

The **Full format** (72 bits) includes every field needed for online learning: weight, target neuron, delay, fatigue state, metaplastic consolidation, and pre-/post-synaptic trace values. The **Inference format** (49 bits) omits learning-specific fields for networks that require only forward-pass execution. The **Compact format** (20 bits) provides maximum synapse density at the cost of delay and plasticity support—suitable for large inference-only layers. The **FACTOR format** (35 bits) implements low-rank factored weight matrices, described below.

5.2 FACTOR Low-Rank Representation

The FACTOR synapse format stores weights as a low-rank factorisation. Rather than storing the weight w_{ij} directly, the format stores indices into two factor matrices $\mathbf{A}$ (size $M \times R$)

Table 4: N3 synapse word formats.

Format	Bits	Density	Fields
Full	72	1×	weight(8b), target(12b), delay(8b), fatigue(4b), meta(3b), traces(8b), reserved
Inference	49	1.5×	weight(8b), target(12b), delay(8b), control(21b)
Compact	20	3.6×	weight(8b), target(12b)
FACTOR	35	2.1×	factor_idx(16b), factor_addr(10b), metadata(9b)

and $\mathbf{B}$ (size $R \times N$), where R is the rank:

$$w_{ij} = \sum_{r=1}^{R} A_{ir} \cdot B_{rj} \tag{14}$$

The factor matrices are stored in L2 shared memory (per-tile). At spike delivery time, the hardware fetches the relevant row of $\mathbf{A}$ and column of $\mathbf{B}$, performs the dot product in Equation (14), and delivers the reconstructed weight to the neuron accumulator. For networks where the weight matrix has low effective rank (common in learned representations), FACTOR achieves 2–8× compression relative to the Full format, with the compression ratio depending on rank R and the matrix dimensions. FACTOR learning is supported via the `STORE_A` and `STORE_B` learning opcodes (Section 6), which update individual entries of the factor matrices.

5.3 Variable-Precision Weights

Weight precision is configurable per synapse group from 1 to 16 bits (1, 2, 4, 8, or 16 bit). At 1-bit precision, synapses store only $\{+1, -1\}$ indicators; at 16-bit, they provide near-floating-point resolution for fine-grained weight tuning. Weight packing is dense: four 4-bit weights share a single 16-bit word, doubling effective synapse density relative to 8-bit. The packing format is little-endian within each word, with the synapse index determining the sub-word offset.

5.4 Synaptic Fatigue

Each synapse in the Full format maintains a 4-bit fatigue counter. Repeated activation within a short window decrements the effective weight:

$$w_{\text{eff}} = w \cdot (1 - \text{fatigue}/15) \tag{15}$$

Fatigue increments by a configurable step (1–4) on each spike delivery and decays exponentially toward zero when the synapse is inactive, with a configurable decay rate ($\tau_{\text{fatigue}} \in \{1, 2, 4, 8, 16, 32\}$ timesteps). This mechanism captures synaptic depression—the biological phenomenon where repeatedly activated synapses temporarily weaken—without requiring learning engine intervention. At maximum fatigue (15), the effective weight is zero, providing automatic short-term depression.

5.5 Configurable Reverse Lookup

The reverse lookup table, used by the learning engine to identify which presynaptic neurons contributed to a postsynaptic spike, supports three configurable fanin sizes: 32, 64, or 128 presynaptic neurons per postsynaptic neuron. Runtime selection via a mode register allows the same hardware to serve networks with different connectivity densities. The lookup table is stored in the synapse index region of L1 (8 KB, Table 1) and is populated during network configuration.

6 Learning and Plasticity

The learning system is N3's most substantial architectural advance. Where N2 provided a single global learning engine with 16 opcodes, N3 distributes **16 independent learning accelerators** (one per tile), each with a **28-opcode ISA** and a **four-stage pipeline** (Figure 4). This eliminates the cross-chip bottleneck that limits plasticity throughput in prior architectures.

6.1 Per-Tile Learning Accelerators

Each tile's learning accelerator processes plasticity updates for its 8 cores independently. The four-stage pipeline consists of: (1) trace fetch and eligibility computation, (2) reward modulation, (3) weight update computation, and (4) writeback with bounds checking and metaplastic consolidation update. At full throughput, one synapse is updated per cycle per tile, yielding 16 synapse updates per cycle chip-wide. At 62.5 MHz, this corresponds to 1 billion synapse updates per second across the full chip.

Each learning accelerator has access to the tile's shared L2 for factor matrix updates and to the 16-channel neuromodulation bus. The accelerator operates on an 80-register file (20 per thread × 4 threads), shared with the neuron engine. Four program regions of 256 instructions each handle LTD (long-term depression), LTP (long-term potentiation), reward modulation, and custom learning rules. Programs are stored in the microcode region of L1 and can be updated at runtime via the host interface.

6.2 Learning ISA (v3.5)

The v3.5 learning ISA extends N2's 16 opcodes to 28:

The 12 new opcodes (`MULACC` through `STORE_FATIGUE`) provide direct hardware access to the plasticity subsystems that are unique to N3: metaplastic consolidation (`STORE_M`),

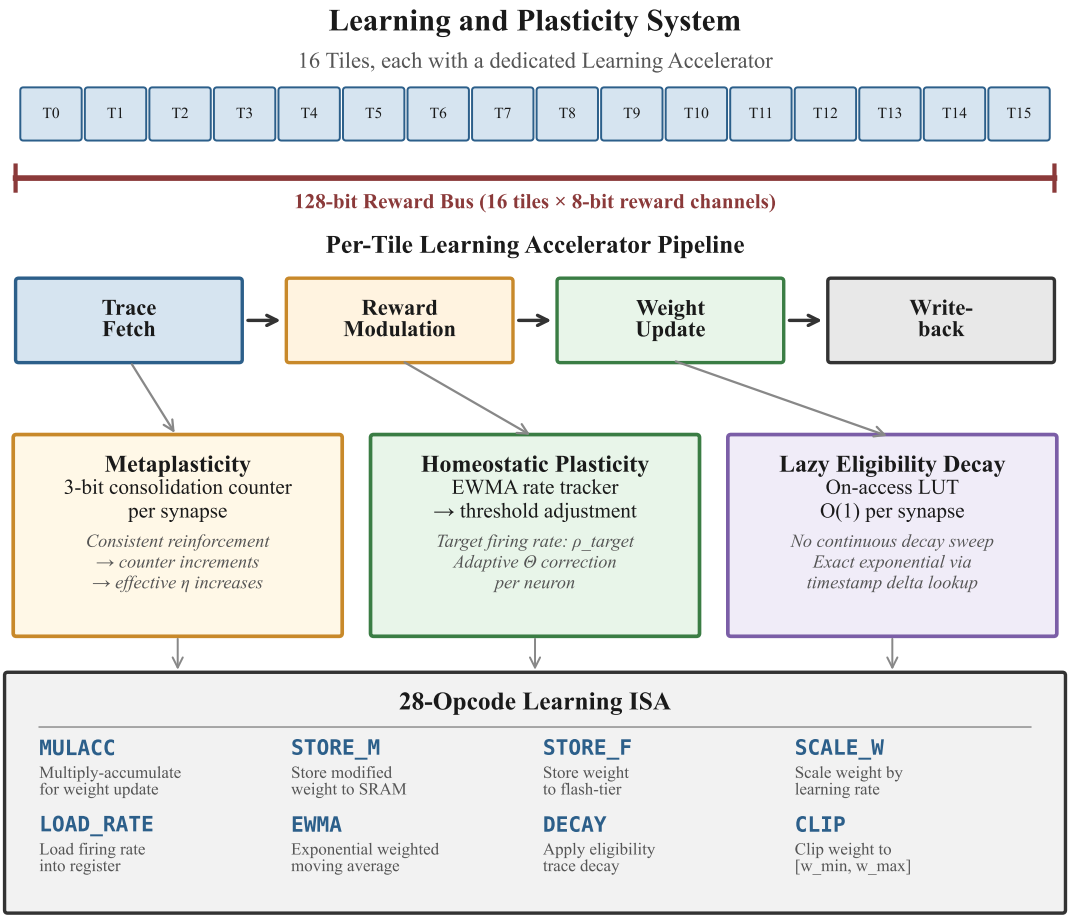

Figure 4: Learning and plasticity system architecture. Each tile contains a dedicated learning accelerator with a four-stage pipeline (trace fetch, reward modulation, weight update, writeback). Sixteen 8-bit neuromodulation channels per tile enable hierarchical credit assignment. Hardware metaplasticity (3-bit consolidation) and homeostatic plasticity (EWMA rate tracking) operate alongside the programmable learning ISA. The lazy eligibility decay mechanism eliminates per-timestep trace scans for inactive synapses.

Table 5: N3 learning ISA opcodes (v3.5). New opcodes marked with $*$.

Opcode	Description
ADD, SUB, MUL, DIV	Arithmetic on learning registers
CLAMP	Saturating clamp to bounds
LOAD, STORE	Register $\leftrightarrow$ memory
SKIP_GT, SKIP_LT	Conditional skip (next instr.)
ABS, NEG	Absolute value, negate
RNG	Pseudorandom number (LFSR)
MULACC*	Multiply-accumulate (fused)
STORE_M*	Write metaplastic consolidation field
STORE_F*	Write FACTOR matrix entries
SCALE_W*	Scale weight by fixed-point factor
LOAD_RATE*	Read homeostatic firing rate
STORE_A*, STORE_B*	Write low-rank factor matrices
LOAD_REWARD*	Read neuromodulation channel
DECAY_E*	Explicit eligibility decay
CMP_RATE*	Compare firing rate to target
LOAD_FATIGUE*	Read fatigue counter
STORE_FATIGUE*	Write fatigue counter

factor matrix updates (`STORE_A`, `STORE_B`, `STORE_F`), homeostatic rate feedback (`LOAD_RATE`, `CMP_RATE`), neuromodulation (`LOAD_REWARD`), fatigue (`LOAD_FATIGUE`, `STORE_FATIGUE`), and efficiency primitives (`MULACC`, `SCALE_W`, `DECAY_E`).

6.3 16-Channel Neuromodulation

Each tile provides a 128-bit reward bus carrying 16 independent 8-bit neuromodulation channels. Per-neuron reward source selectors (2-bit field in the parameter group) choose between four modes: global broadcast (channel 0 replicated to all neurons), tile-local channels (0–15, selected by parameter group), local neuron output (a neighbouring neuron's spike rate serves as the reward signal), or a channel select register (host-writable for external reward injection). Multi-channel reward enables hierarchical credit assignment for reinforcement learning tasks, where different neuron populations respond to different reward signals—for example, a cortical column model where layers 2/3 and layers 5/6 receive different dopaminergic inputs.

6.4 Hardware Metaplasticity

Metaplasticity—the plasticity of plasticity—prevents runaway Hebbian learning by making the effective learning rate dependent on a synapse's recent plasticity history [15]. N3 implements this in silicon with a 3-bit consolidation field per synapse (in the Full format):

$$\eta_{\text{eff}} = \eta \cdot (1 + \alpha_{\text{meta}} \cdot \text{consolidation}) \tag{16}$$

When a synapse undergoes consistent reinforcement (weight updates of the same sign on consecutive learning epochs), its consolidation counter increments (up to 7), progressively increasing the effective learning rate for further reinforcement and resistance to subsequent depression. Conversely, inconsistent reinforcement (sign reversal) resets the counter to zero. The scaling factor α_{meta} is configurable per parameter group (typical range: 0.1–0.5 in 4-bit fixed-point).

This mechanism stabilises learned representations without software intervention, at a cost of only 3 bits per synapse. The consolidation counter is updated by the learning accelerator's writeback stage and is accessible to learning programs via the `STORE_M` opcode for custom consolidation policies.

6.5 Homeostatic Plasticity

Biological networks maintain stable firing rates through homeostatic mechanisms [16]. N3 implements this via exponentially weighted moving average (EWMA) firing-rate tracking per neuron group:

$$\text{rate}[t] = \text{rate}[t-1] - (\text{rate}[t-1] \gg \tau_h) + (s[t] \cdot (255 \gg \tau_h)) \tag{17}$$

where τ_h is the EWMA time constant (3-bit, selecting $\gg$ shifts of 1–8, corresponding to effective time constants of 2–256 timesteps). At epoch boundaries (configurable via a period register), the hardware compares the measured rate against a target firing rate (configurable per parameter group, 8-bit). If the rate exceeds the target, the threshold increases proportionally; if it falls below, the threshold decreases:

$$\theta[t] = \theta[t] + \alpha_h \cdot (\text{rate}[t] - \text{rate}_{\text{target}}) \tag{18}$$

where α_h is the homeostatic scaling factor (4-bit fixed-point). The learning ISA's `LOAD_RATE` opcode exposes the measured rate to custom learning programs, and `CMP_RATE` performs the comparison in a single cycle, enabling learning rules that incorporate rate feedback.

6.6 Lazy Eligibility Decay

In prior architectures, eligibility traces decay every timestep, requiring an $O(N)$ scan over all synapses. N3's lazy eligibility decay eliminates this cost. When a synapse is accessed (for either spike delivery or learning), the hardware computes the correct decayed value from a pre-computed lookup table indexed by the elapsed time since last access:

$$e_{\text{eff}}[t] = e[t_{\text{last}}] \cdot \text{decay\_table}[t - t_{\text{last}}] \tag{19}$$

The decay table stores 256 entries of pre-computed $\lambda^{\Delta t}$ values for the configured trace decay rate λ, in 8-bit fixed-point. The timestamp t_{last} is stored in 8 bits per synapse (supporting up to 255 timesteps of inactivity; longer gaps saturate to full decay). Synapses that are never accessed incur zero decay computation. For sparse networks where only a fraction

of synapses are active per timestep, this reduces learning overhead by 10–100× compared to the naive $O(N)$ approach.

6.7 FACTOR Learning

The FACTOR synapse format (Section 5) supports online learning via the `STORE_A` and `STORE_B` opcodes, which write individual entries of the factor matrices $\mathbf{A}$ and $\mathbf{B}$ stored in L2. A learning program can compute gradient updates for the low-rank factors and apply them in place:

$$A_{ir} \leftarrow A_{ir} + \eta \cdot \delta_j \cdot B_{rj} \tag{20}$$

$$B_{rj} \leftarrow B_{rj} + \eta \cdot \delta_j \cdot A_{ir} \tag{21}$$

where δ_j is the error signal for postsynaptic neuron j. The `STORE_F` opcode provides a combined write that updates both factors atomically, preventing inconsistency during concurrent reads.

6.8 Learning Rule Assembly Example

The following example demonstrates a three-factor reward-modulated STDP rule implemented using the v3.5 learning ISA. This rule computes eligibility from pre- and post-synaptic traces, modulates by a reward signal, and applies the update with metaplasticity scaling:

Listing 1: Three-factor STDP learning rule in N3 ISA v3.5.

```
; Three-factor reward-modulated STDP
; LTD program region
    LOAD R0, x1           ; pre-synaptic trace
    LOAD R1, y1           ; post-synaptic trace
    MULACC R2, R0, R1     ; eligibility = pre * post
    LOAD_REWARD R3        ; reward signal (channel 0)
    MUL R4, R2, R3        ; modulated = elig * reward
    SCALE_W R5, R4        ; scale by learning rate
    CLAMP R5, -128, 127   ; saturate to weight range
    STORE R5              ; write weight update
    STORE_M R5            ; update consolidation
    HALT
```

This 10-instruction program executes in 10 cycles (one instruction per cycle) per synapse. With the four-stage pipeline processing 8 cores per tile, a tile with 32,768 synapses per core completes one full learning pass in approximately $32{,}768 \times 10/62.5 \times 10^6 \approx 5.2\,\text{ms}$—well within a typical 10 ms biological timestep budget.

7 Network-on-Chip

7.1 Three-Level Hierarchical Design

N3's NoC comprises three levels matched to the physical hierarchy (Figure 5):

1. **Intra-tile (L1 NoC):** An 8-core asynchronous handshake mesh connects cores within each tile. Four-phase handshake protocols (request-acknowledge with return-to-zero) consume zero dynamic power when idle—spikes only draw current when they transit. A routing tile at the centre of each mesh provides format conversion and spike buffering via a 256-deep FIFO in the ASIC target (64-deep on FPGA due to BRAM constraints). The intra-tile router supports unicast, multicast (up to 8 destinations within the tile), and broadcast modes. Worst-case intra-tile latency is 3 hops (corner to corner through the central router).
2. **Inter-tile (L2 NoC):** A hierarchical fat tree connects the 16 tile routers. Eight express links per tile provide configurable bypass paths for high-traffic routes, reducing worst-case hop count from 7 (tree path between maximally distant tiles) to 1 (direct express link). Minimal adaptive routing with XY/YX fallback on congestion, combined with virtual channel class bits (2-bit, 4 classes) for deadlock freedom, balances throughput and determinism. The inter-tile packet format carries a 48-bit payload (source tile:4, source core:3, destination tile:4, destination core:3, multicast group:8, spike data:24, priority:2). Average inter-tile latency is 2–3 hops without express links and 1–2 hops with express links configured for the active network topology.
3. **Off-chip (L3 NoC):** CXL 2.0 coherent links and 8 AER links provide multi-chip connectivity. Spike compression (DELTA, BURST, and ADAPTIVE encoding modes) reduces off-chip bandwidth by 2–8× depending on spike pattern regularity. DELTA encoding transmits only the difference from the previous spike address (effective for spatially correlated spike patterns). BURST encoding compresses consecutive spikes from the same source into a count-address pair. ADAPTIVE dynamically switches between DELTA and BURST based on a running efficiency estimate.

7.2 Asynchronous-Synchronous Hybrid

The cores operate synchronously at 62.5 MHz (FPGA) or the target ASIC frequency, while the NoC routers use asynchronous four-phase handshake signalling. This hybrid approach provides two key benefits. First, idle routers draw near-zero dynamic power—only the clock-gated synchronous cores consume power during neuron computation, and the NoC activates only when spikes are in flight. Second, the asynchronous routers naturally accommodate clock domain crossings between tiles, simplifying physical design for large die implementations where clock skew across the projected multi-hundred mm^2 die would otherwise require extensive buffering.

Tile adapter modules at the synchronous-asynchronous boundary handle conversion. The transmit adapter samples synchronous spike FIFO outputs onto asynchronous request-acknowledge signals; the receive adapter synchronises incoming asynchronous spikes into the core's clock domain via a two-flop synchroniser with metastability hardening. The adapters add 2–3 cycles of latency per boundary crossing.

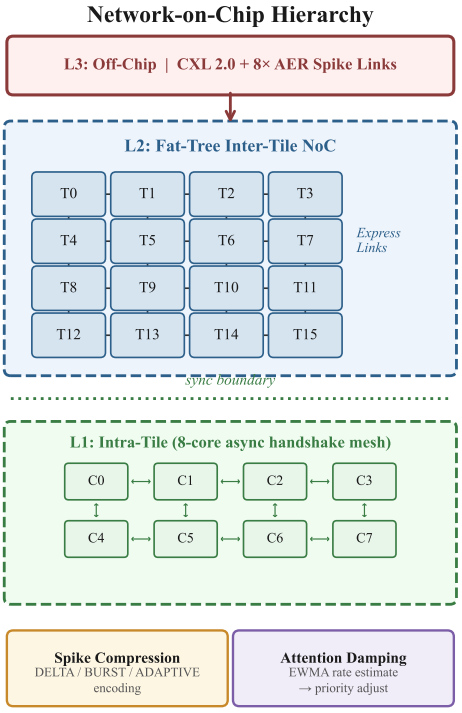

Figure 5: N3 network-on-chip topology. Intra-tile: 8-core asynchronous mesh with central routing tile. Inter-tile: hierarchical fat tree with 8 configurable express bypass links per tile. Off-chip: CXL 2.0 coherent and 8 AER links with spike compression.

7.3 Express Links

Each tile provides 8 configurable express links that bypass intermediate routers. Express links are programmed at network configuration time with source-destination tile pairs for high-traffic routes. For a 16-tile chip, express links reduce worst-case inter-tile latency from 7 hops (tree path) to 1 hop (direct link), and average-case latency from 3–4 hops to 1–2 hops. The configuration registers support dynamic reprogramming, enabling the host to reconfigure express link assignments when the active virtual network changes during TDM slot transitions.

Each express link provides a dedicated 48-bit datapath with its own 16-deep FIFO buffer. When the express FIFO is full, the spike falls back to the standard fat-tree path. The 8 links per tile are sufficient to cover the 4–6 highest-traffic routes in typical SNN topologies (feedforward layers, recurrent connections, inhibitory projections).

7.4 Multicast and Attention

Each tile supports 256 multicast groups of up to 32 destinations each. A spike tagged with a multicast group ID is replicated and delivered to all group members in a single routing operation, avoiding the $O(N)$ unicast overhead of fan-out patterns. The multicast table (256 entries $\times$ 32-bit destination mask = 1 KB) is stored in the routing tile's local SRAM.

Attention damping (feature #62a) provides priority-based spike routing. Each tile maintains an EWMA estimate of its outbound spike rate (8-bit, updated every 256 timesteps). When the rate exceeds a configurable threshold, outbound spike priority is dynamically reduced by decrementing the 2-bit priority field, allowing tiles with lower activity to claim more NoC bandwidth. A per-tile boost budget (4-bit counter, replenished at epoch boundaries) provides transient high-priority access for bursty patterns, preventing starvation of tiles that are briefly active after long quiescence.

8 Efficiency and Virtualisation

8.1 Time-Division Multiplexing

TDM enables N3 to time-share physical cores across multiple virtual networks. At each TDM slot, the hardware loads a virtual network's context from L3 into L1/L2 via DMA scatter-gather, executes a configurable number of timesteps, then saves modified state back. The **dirty context tracking** mechanism (feature #61) maintains a 12-bit dirty vector per core, indicating which of the approximately 12 SRAM banks were modified. Only dirty banks are saved, reducing context-switch DMA traffic by 3–10$\times$ for typical networks where only a subset of neuron groups are active per timestep.

Shadow SRAM banks (feature #60a) provide double-buffering for zero-stall context switching: while one set of banks serves the active computation, the DMA engine loads the next context into the shadow set. Combined with **TDM**

pre-wake (feature #62b), which wakes a tile during the DMA load phase of the next batch, context-switch latency is hidden behind computation.

At maximum TDM depth, 128 physical cores × 32 TDM slots × 1,024 neurons yields 4,194,304 virtual neurons. At 4,096 neurons per core (with parameter groups), a single TDM slot already provides 524,288 neurons—sufficient for most current SNN benchmarks.

8.2 ANN Mode Integration

N3's INT8 ANN mode (Model 1, Section 4) enables each core to operate as a conventional multiply-accumulate unit, supporting hybrid SNN/ANN architectures on a single chip without off-chip data transfer.

8.3 Power Management

N3 implements power management at two granularities:

Per-tile power gating (feature #64). A 7-state FSM manages each tile's power domain: ACTIVE (full operation), DROWSY (clock-gated, state retained in SRAM), SLEEP (power-gated, state checkpointed to L3), WAKE_DMA (loading context from L3), WAKE_READY (context loaded, awaiting first spike), and two transition states (DROWSY_TO_SLEEP and SLEEP_TO_WAKE) that handle the multi-cycle power-rail ramp and retention-cell transfer. Wake-on-spike triggers transition from SLEEP to ACTIVE when an incoming spike targets a powered-down tile. The transition latency is: DROWSY→ACTIVE in 1 cycle (clock un-gate), SLEEP→ACTIVE in 50–200 cycles (DMA load, depending on context size).

Per-pipeline-stage clock gating (feature #65). Four independent latch-based integrated clock gating (ICG) cells gate the synapse delivery, neuron update, learning, and writeback pipeline stages independently. When a core has no spikes to deliver but neurons to update, only the neuron update stage consumes dynamic power. The ICG cells use the standard latch-and-gate topology to prevent glitches on the gated clock. Activity signals propagate one cycle ahead via the pipeline control logic, ensuring the ICG opens before the data arrives.

8.4 Approximate Computing

A per-core quality register (feature #42) enables approximate neuron updates. Neurons whose membrane potential is further than a configurable distance d_{approx} from the firing threshold are skipped during the update phase, saving computation for neurons that are unlikely to spike. The approximation criterion is:

$$\text{skip}(i) = \begin{cases} 1 & \text{if } |v_i[t-1] - \theta_i| > d_{\text{approx}} \text{ and activity}[i] = 0 \\ 0 & \text{otherwise} \end{cases} \tag{22}$$

where activity$[i]$ is the activity bitmap flag indicating whether neuron i received input this timestep. The quality register is configurable per virtual network, enabling accuracy-power trade-offs at the application level. Setting $d_{\text{approx}} = 0$ disables approximation.

9 Reliability and Determinism

9.1 ECC Scrubbing

All L1 and L2 SRAMs are protected by SEC-DED (single-error correcting, double-error detecting) Hamming codes. A 4-state round-robin scrubbing FSM (feature #67) continuously reads, checks, and repairs SRAM contents in the background. The four states are: IDLE (waiting for scrub timer), READ (fetch next SRAM word), CHECK (ECC syndrome computation), and REPAIR (correct single-bit error or flag double-bit error). Scrub rate is configurable via a period register (8-bit, selecting intervals from 256 to 65,536 cycles); the FSM interleaves scrub reads with normal accesses via an arbiter to avoid stalling the neuron pipeline. At the default scrub rate (every 4,096 cycles at 62.5 MHz), a full 96 KB L1 is scrubbed in approximately 100 ms.

9.2 Deterministic Mode

Full-chip determinism (feature #59a) is essential for debugging and validation. When enabled, deterministic mode provides three guarantees: (1) all LFSR-based noise generators are seeded from a host-provided 32-bit seed, producing identical pseudorandom sequences across runs; (2) the GALS (globally asynchronous, locally synchronous) clock domain crossing is bypassed, forcing all tiles to run from a single synchronous clock; and (3) barrier synchronisation ensures all cores complete timestep t before any core begins timestep $t+1$. Together, these guarantees produce bit-identical results across runs, enabling differential debugging against the cycle-accurate CPU simulator.

The barrier synchronisation is implemented via a tree reduction: each tile asserts `tile_done` when all 8 cores complete the current timestep, and a 4-level reduction tree (matching the fat-tree NoC topology) generates a global `chip_done` signal that releases the next timestep. In non-deterministic mode, the barrier is disabled and each tile advances independently (GALS operation), improving throughput at the cost of non-reproducible spike ordering.

9.3 Performance Counters and Interrupts

Each tile provides 32 hardware performance counters (feature #59c), each 64-bit, totalling 512 counters chip-wide.

Counters track: spike counts (inbound, outbound, dropped), synapse updates (by format), learning cycles (by program region), stall cycles (pipeline, NoC, DMA), NoC congestion events (per-link, per-virtual-channel), power-gating transitions (ACTIVE→DROWSY, DROWSY→SLEEP, wake events), and ECC correction events (single-bit, double-bit). All counters are readable via the AXI4-Lite host interface and can be configured to trigger interrupts on overflow or threshold crossing.

A 16-source priority-encoded interrupt controller (feature #60c) with auto-clear supports DMA completion, ECC double-bit error, learning epoch completion, TDM slot transition, performance counter overflow, power-state transitions, timestep completion, and 9 software-triggered events. The interrupt controller supports both edge-triggered and level-sensitive modes, with per-source masking.

10 SDK and Software Stack

10.1 Overview

The `neurocore` SDK (v3.7.0) provides a complete software stack for developing, simulating, compiling, and deploying spiking neural networks on Catalyst hardware. The SDK comprises 88 Python modules with 3,091 unit tests, achieving greater than 95% code coverage across all public APIs.

10.2 Three Backends

The SDK provides three interchangeable backends with a common API:

1. **CPU Simulator.** Cycle-accurate reference implementation that models every register, SRAM, and pipeline stage of the hardware. Used for correctness validation against RTL simulation and as the ground truth for the GPU backend's numerical accuracy. Typical throughput: 50–500 timesteps per second for a single-tile network, depending on neuron count and connectivity.
2. **GPU Simulator.** PyTorch-based batch-parallel implementation that trades cycle accuracy for 100–1,000× speedup. Neuron updates, synapse delivery, and learning are expressed as tensor operations, enabling GPU acceleration and automatic differentiation for surrogate-gradient training. The GPU backend reproduces CPU backend results within quantisation bounds (± 1 LSB at 24-bit) for all 8 neuron models and all learning opcodes.
3. **FPGA Backend.** Deploys compiled networks to Catalyst hardware on AWS F2 via PCIe MMIO. The backend handles weight quantisation, SRAM layout, CSR programming, and real-time spike injection/collection. Communication uses a ring-buffer protocol over the AXI4-Lite interface: the host writes stimulus spikes to a 4 KB input buffer and reads output spikes from a 4 KB output buffer, with doorbell registers for synchronisation.

A network compiled with the CPU backend can be deployed on FPGA by changing a single constructor argument (`backend="fpga"`), with the compiler automatically handling weight quantisation, memory layout, and CSR register programming.

10.3 Feature Parity Assessment

A systematic assessment identified 155 features in Intel's Loihi 2 specification. Of these, 152 are fully implemented in the SDK. The three remaining features—physical multi-chip spike routing, inter-chip barrier synchronisation, and hardware breakpoint debug—require physical multi-chip links that are not available on the single-tile FPGA validation platform. All 152 implemented features have corresponding test coverage in the 3,091-test suite.

10.4 Network Builder API

The SDK provides a hierarchical network builder API:

Listing 2: Network construction and deployment example.

```
from neurocore import Population, Connection
from neurocore import LearningRule, Simulator

# Define populations
inp = Population(700, model="input")
hid = Population(1024, model="alif",
                 params={"tau_adapt": 50})
out = Population(35, model="graded")

# Connect with learning
rule = LearningRule()
rule.assemble_ltd("""
    LOAD R0, x1           ; pre trace
    LOAD R1, y1           ; post trace
    MULACC R2, R0, R1     ; eligibility
    LOAD_REWARD R3        ; reward
    MUL R4, R2, R3        ; modulated
    SCALE_W R5, R4        ; scale
    STORE R5              ; write weight
    STORE_M R5            ; metaplasticity
    HALT
""")
conn = Connection(inp, hid, format="full",
                  learning_rule=rule)

# Simulate
sim = Simulator(backend="gpu")
sim.compile([inp, hid, out], [conn])
sim.run(timesteps=250)

# Deploy to FPGA
sim_hw = Simulator(backend="fpga")
sim_hw.compile([inp, hid, out], [conn])
sim_hw.run(timesteps=250)
```

10.5 Compiler Pipeline

The compiler transforms a high-level network description into hardware-ready configuration through four stages:

1. **Placement:** Assigns populations to cores and tiles, minimising inter-tile spike traffic. The placer uses a greedy bin-packing algorithm with connection-weight-based affinity scoring.
2. **CSR Allocation:** Maps neuron parameters to parameter groups, assigns synapse formats, and generates the per-core

configuration register (CSR) values. The allocator validates that each core's SRAM budget (Table 1) is not exceeded and reports an error if the network is too large for the target hardware.

3. **SRAM Budget Check:** Verifies that the total L1 usage (neuron state + traces + synapse index + weights + microcode + queues) fits within 96 KB per core. If the budget is exceeded, the compiler suggests mitigation strategies: reduce neuron count, use Compact synapse format, or enable 16-bit precision.
4. **Routing:** Generates spike routing tables and express link assignments. For multi-tile networks, the router computes shortest paths on the fat-tree topology and assigns express links to the highest-traffic routes.

10.6 Analysis Tools

The SDK provides post-simulation analysis tools: raster plots (spike times vs. neuron ID), firing rate histograms, inter-spike interval (ISI) distributions, cross-correlation matrices, weight evolution traces, learning convergence curves, and per-neuron state monitors (membrane potential, adaptation variable, traces over time). All analysis functions accept both CPU/GPU simulation results and FPGA-collected spike data, enabling direct comparison between simulation and hardware.

11 FPGA Implementation

11.1 Target Platform

We validate N3 on a Xilinx VU47P FPGA hosted on an AWS F2 instance (f2.6xlarge). The FPGA resource budget supports a single tile of 8 cores—the full 128-core chip requires ASIC fabrication. The AXI clock operates at 250 MHz; a Xilinx MMCME4 PLL generates the 62.5 MHz neuromorphic clock via divide-by-4. Clock domain crossing between AXI and neuromorphic domains uses two-stage synchronisers with registered false-path constraints in the timing closure flow.

The F2 instance provides PCIe Gen3 $\times 16$ connectivity between the host CPU and the FPGA. The Shell (AWS-provided infrastructure) occupies approximately 20% of FPGA resources; the remaining 80% is available for the custom logic (CL). Our 8-core tile CL uses a modest fraction of the available resources, as detailed below.

11.2 Resource Utilisation

Table 6: N3 FPGA resource utilisation (8-core tile, VU47P).

Resource	Used	% Available
BRAM36	712	19.9%
BRAM18	575	8.0%
URAM	16	1.5%
DSP48	98	3.6%

The modest resource utilisation—particularly the 3.6% DSP and 19.9% BRAM36 usage—confirms that the 8-core tile is well within the FPGA's capacity. BRAM36 is the binding constraint: each core's L1 SRAMs are inferred as BRAM36 primitives (approximately 89 per core $\times$ 8 cores = 712). Scaling to the full 128 cores (16 tiles) would require approximately $16\times$ the BRAM, exceeding the VU47P's 3,564 BRAM36 capacity; this motivates the ASIC target.

11.3 Timing Closure

The N3 FPGA build (v27) achieves timing closure at 62.5 MHz with:

- **Post-place WNS:** +0.540 ns (significant positive slack)
- **Final WNS:** 0.000 ns (met exactly after routing)
- **Final WHS:** -0.089 ns (89 ps hold violation, functionally benign on FPGA)

The build converged in 2 hours 47 minutes on an r7a.2xlarge instance (8 vCPU, 64 GB RAM). The 89 ps hold violation is on a path between the MMCME4 output and a synchroniser flip-flop; at 62.5 MHz (16 ns period), this margin is absorbed by the FPGA's internal hold-time guardband and does not affect functional correctness.

11.4 Build Narrative: 27 Iterations to Silicon Validation

The path from first synthesis to full hardware validation required 27 FPGA builds spanning four months. This section documents the key bugs encountered and their resolutions, as a reference for future neuromorphic FPGA efforts.

v1–v4: Clock generation failure. The initial builds used a `BUFGCE_DIV` primitive to generate the 62.5 MHz neuromorphic clock from the 250 MHz AXI clock. All four builds synthesised successfully but failed to load onto the FPGA—the AWS Shell reported a clock frequency mismatch. The root cause was that `BUFGCE_DIV` does not provide the frequency feedback that the Shell's clock management logic requires. **Fix:** Replace `BUFGCE_DIV` with an `MMCME4_ADV` PLL configured for divide-by-4 with explicit frequency output.

v5–v19: Incremental feature integration. Builds v5 through v19 progressively added neuromorphic features (neuron models, learning engine, NoC router, performance counters) with successful FPGA loads but limited functional testing. Each build was verified against simulation for the newly added feature before proceeding.

v20: DeviceId out of range. Build v20 implemented the complete 8-core tile with all N3 features. The build synthesised and loaded successfully, but the FPGA was invisible to the host—no PCIe device appeared. The root cause was the

PCIe Device ID: we had set it to `0xF330`, but AWS F2 requires Device IDs in the range `0xF000–0xF0FF` (Vendor ID `0x1D0F`). **Fix:** Change Device ID to `0xF030`.

v21: Hold violations. With the Device ID corrected, v21 loaded and appeared on the PCIe bus, but neuron computation produced incorrect results. Timing analysis revealed hold violations on paths between the neuromorphic clock domain and the AXI clock domain. The CDC (clock domain crossing) synchronisers were correctly placed, but the timing constraints did not include false-path declarations for these crossings. **Fix:** Inject CDC false-path constraints via Tcl scripts in the Vivado build flow (not XDC files, which the F2 flow overwrites).

v22–v23: CDC constraint refinement. Builds v22–v23 iterated on the false-path constraint set, resolving residual hold violations and achieving positive WHS for the first time.

v24: SLR pblock strategy. Build v24 introduced Super Logic Region (SLR) pblock constraints to confine the 8-core tile to a single SLR die, eliminating inter-SLR timing paths. This achieved WHS = +0.010 ns and passed 18/19 hardware tests. The single failure was the RUN command: issuing a multi-timestep run caused the system to hang. Investigation revealed that the `ts_done_latched` signal was implemented as a level (sustained high while timestep was complete) rather than a pulse (single-cycle high). The AXI state machine waited for a rising edge that never came after the first timestep. **Fix:** Convert `ts_done_latched` from level to pulse using a registered edge detector.

v25: Multi-timestep skipping. Build v25 fixed the `ts_done_latched` bug, enabling single-timestep runs. However, multi-timestep runs (e.g., run 100 timesteps) produced results as if only 1 timestep had executed. The root cause was an edge-detection synchroniser in the neuromorphic-to-AXI clock crossing: the synchroniser sampled the pulse too late, missing intermediate timestep completions. **Fix:** Add a second synchroniser stage with registered output and use the synchronised pulse to increment a timestep counter.

v26: 18/19 pass. Build v26 achieved 18/19 test pass rate at 15,000 timesteps per second. The single failure was the `chip_cfg` readback test: the host read stale configuration values after a write. The root cause was a missing write-readback path in the chip configuration register file. **Fix:** Add a combinational readback mux from the write port to the read port, with a one-cycle registered delay for timing closure.

v27: All pass. Build v27 fixed the `chip_cfg` readback, added the custom ISA neuron engine (Model 7), and corrected the DVFS default (which had been enabled, causing frequency scaling that confused the timestep counter). Result: **19/19 hardware tests pass, 14,512 timesteps per second**. The final AFI is `agfi-0df16698ef37c59d9`.

Design decisions. Three design decisions were critical to timing closure. First, all neuromorphic SRAMs use **BRAM inference** (not instantiation), allowing Vivado to choose optimal BRAM primitive sizes and placements. Second, the **SLR pblock** strategy confines the entire 8-core tile to a single SLR, eliminating the 1–2 ns inter-SLR crossing penalty. Third, CDC false-path constraints are **injected via Tcl** (in the `synth_design` and `opt_design` hooks), not via XDC files, because the F2 Shell build flow overwrites user XDC files with its own constraints.

11.5 Hardware Validation

The FPGA validation suite comprises 4 test suites and 19 individual tests:

Table 7: N3 FPGA hardware validation results (v27).

Suite	Tests	Pass
AXI Loopback	VERSION, CORE_COUNT, SCRATCH, STATUS, ERROR_STATUS, chip_cfg, MODE	7/7
N3 Features	error_status, chip_cfg, perf_counters, neuron_probe, stimulus→spike, multi-core, trace	7/7
Spike Chain	timestep delta, chip idle, spike count	3/3
Cross-Core	cross-tile routing (C0=3, C1=2 spikes)	2/2
Total		**19/19**

Measured throughput on the 8-core tile is **14,512 timesteps per second** (68.9 μs per timestep), processing 32,768 neurons per timestep (8 cores $\times$ 4,096 neurons). This represents a 1.8$\times$ improvement over N2's 7,886 timesteps per second on 16 cores—despite having half the core count, N3 achieves higher throughput through the activity bitmap skip, four-thread pipeline, per-stage clock gating, and parameter group compression.

FPGA energy efficiency. Vivado power analysis reports 1.923 W for the neuromorphic design (N3 tile) and 1.913 W for N2 at the same 62.5 MHz clock. The energy per neuron-timestep is:

$$E_{\text{N3}} = \frac{1.923\,\text{W}}{14{,}512 \times 32{,}768} = 4.04\,\text{nJ/neuron-op} \tag{23}$$

compared to N2's $1.913/(7{,}886 \times 16{,}384) = 14.8$ nJ/neuron-op—a **3.7$\times$ improvement** in per-neuron energy efficiency on the same FPGA. For benchmark inference, the SSC task (250 timesteps) requires $250 \times 68.9\,\mu\text{s} = 17.2$ ms latency and $250 \times 1.923\,\text{W} \times 68.9\,\mu\text{s} = 33.1$ mJ per inference on FPGA. Applying standard FPGA-to-ASIC scaling (10–20$\times$

power reduction [29]), we project 1.7–3.3 mJ per SSC inference at 28 nm—competitive with Loihi 2's estimated energy envelope for comparable workloads.

11.6 Simulation Validation

Prior to FPGA deployment, the N3 RTL was validated against 57 testbenches comprising 1,011 individual tests. The RTL comprises 46 Verilog source files totalling approximately 17,700 lines, with 897 inline assertions covering state machine transitions, SRAM access sequencing, pipeline hazards, and clock domain crossing protocols. All 68 specification features achieve a 10/10 completeness rating (two features—thermal management and runtime precision adaptation—are legitimately excluded as they require physical sensors or SRAM controller redesign respectively). A single testbench (`tb_n3_integrated`, a 32-core integration test) times out in Icarus Verilog simulation due to the simulation scale; this configuration is validated on the physical FPGA.

11.7 Comparison to N1 and N2 FPGA

Table 8: FPGA validation comparison across Catalyst generations.

Metric	N1	N2	N3
Cores	16	16	8
Total neurons	16,384	16,384	32,768
Throughput (ts/sec)	8,690	7,886	14,512
Neuron models	1	5	8 (+ISA)
Learning opcodes	14	16	28
Learning registers	16	16	80
Hardware tests	98	28	19
Simulation tests	168	3,091	1,011
RTL lines	∼5K	∼12K	∼17.7K
Verilog files	18	32	46
Assertions	120	445	897

The key observation is that N3 achieves 2× the neuron count and 1.8× the throughput with half the cores, demonstrating that the architectural efficiency improvements (parameter groups, activity bitmap skip, four-thread pipeline, per-stage clock gating) more than compensate for the reduced core count on FPGA. The growing assertion count (120→445→897) reflects the increasing architectural complexity and our commitment to hardware verification.

11.8 ASIC Characterisation

In parallel with FPGA validation, we conducted ASIC synthesis and place-and-route campaigns using Yosys 0.34 for logic synthesis and OpenLane 2 [31] for physical design, targeting the SKY130A process (`sky130_fd_sc_hd` standard cells). These campaigns serve as a synthesisability proof—demonstrating that the RTL maps cleanly to standard cells and passes physical design rule checks—rather than a tape-out pathway. Commercial ASIC fabrication would require a foundry 28 nm PDK and full sign-off EDA toolchain.

Block-level results (SKY130, 130 nm). Table 9 summarises the three major blocks that completed the OpenLane flow.

Table 9: N3 ASIC block-level synthesis results (SKY130A 130 nm, Yosys 0.34 + OpenLane 2).

Block	Cells	Area (mm^2)	DRC	Status
Router	89,812	6.51	36	Full PnR
Host interface	3,807	0.896	0	Full PnR
Core (synth)	∼1.5M*	—	—	Synth only

*1,045,706 FFs + 2,317,608 pre-ABC gates; ABC timed out. Estimated 1.5M post-optimisation (actual may be 20–30% lower).

The router and host interface completed full place-and-route through GDS. The host interface achieved zero DRC violations—a clean design rule closure. The router's 36 remaining DRC violations are minor routing-level issues fixable with additional iteration. The core completed Yosys synthesis successfully but the ABC logic optimisation pass timed out at the 1-hour limit due to the block's complexity (over 3.3 million pre-optimisation gates). The 1.5M post-ABC estimate is based on typical ABC compression ratios of 40–55% for neuromorphic logic; the actual post-optimisation count may be lower.

N2 vs. N3 comparison. Table 10 compares the N2 and N3 synthesis results, revealing where architectural complexity concentrates.

Table 10: N2 vs. N3 ASIC comparison (SKY130 synthesis, Yosys 0.34).

Metric	N2	N3	Ratio
Router cells	84,299	89,812	1.07×
Core FFs	19,913	1,045,706	52×
Core pre-ABC gates	43,834	2,317,608	53×
Projected GSOPs/J	8.7	57	6.5×

The router grows by only 6.5%, confirming that shared NoC infrastructure scales efficiently. The 52× core growth reflects the 34 new features (parameter groups, 8 neuron models, metaplasticity, homeostatic plasticity, synaptic fatigue, TDM virtualisation) that distinguish N3 from N2's Loihi 2-parity baseline. Despite this complexity increase, the projected energy efficiency improves 6.5× due to the 4× neuron density gain from parameter groups and architectural optimisations that amortise control overhead across more neurons per cycle.

28 nm area projections. We project ASIC die area at 28 nm using geometric technology scaling: $(130/28)^2 \times 0.7 = 15.0\times$ area reduction from SKY130, where the 0.7 factor accounts for routing overhead improvements at advanced nodes. Table 11 summarises the projections.

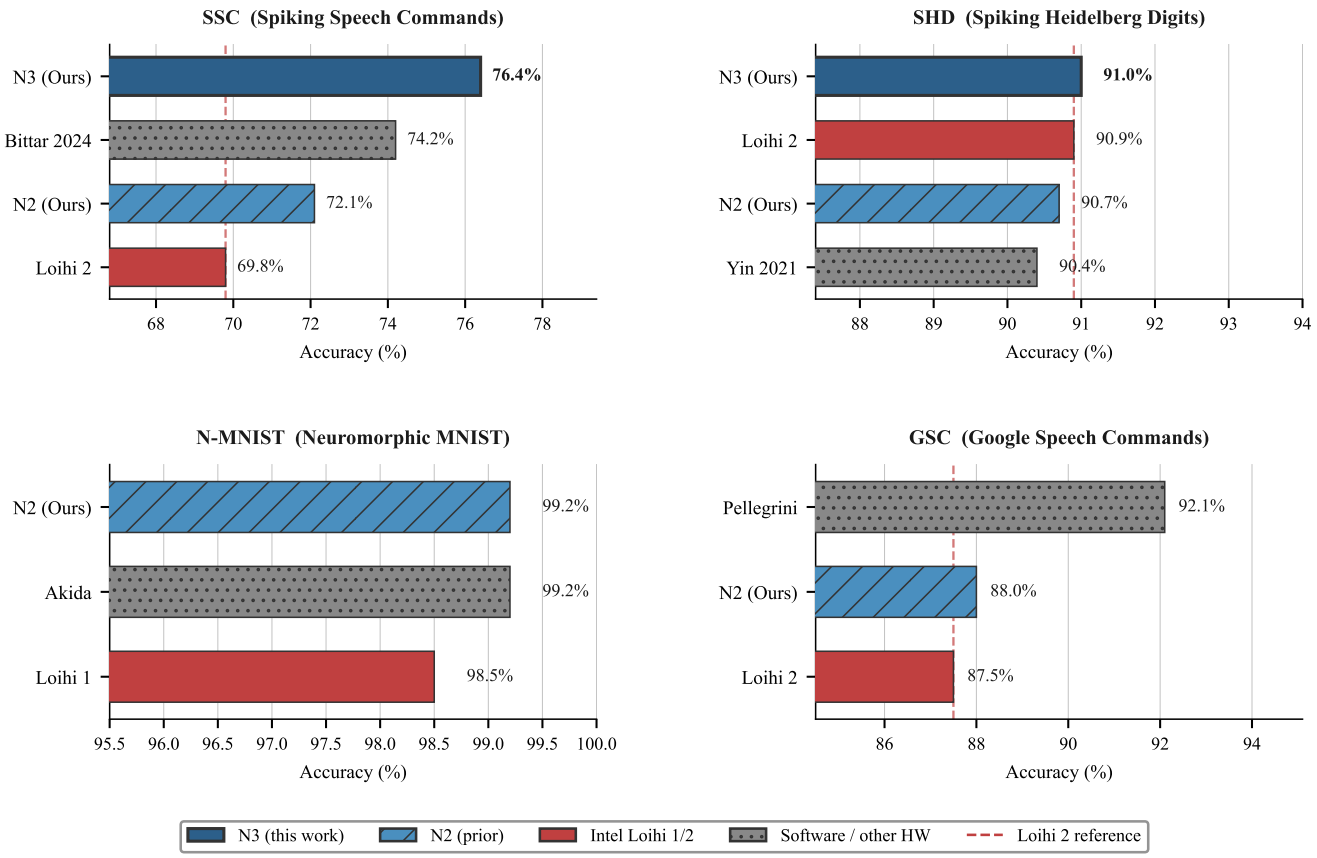

Figure 6: Benchmark comparison across neuromorphic platforms. Left: SSC test accuracy (35-class, N3 achieves new state of the art at 76.4%). Centre-left: SHD test accuracy (20-class, N3 exceeds Loihi 2 at 91.0%). Centre-right: N-MNIST test accuracy (10-class, N2 result matches BrainChip Akida). Right: GSC KWS test accuracy (12-class, N2 exceeds Loihi 2).

Table 11: Projected 28 nm die area (geometric scaling from SKY130).

Configuration	Area (mm^2)	Notes
N3-8 (1 tile)	∼58	8 cores + router + host
N3-128 (full chip)	∼1,070	16 tiles + global NoC + I/O
Loihi 2 (Intel 4)	31	For reference

The projected 1,070 mm^2 full-chip area at 28 nm is large but reflects N3's substantially richer per-core feature set relative to Loihi 2. At Intel 4 (7 nm equivalent), the same scaling would yield approximately 70 mm^2—comparable to Loihi 2's 31 mm^2, with the remaining difference attributable to N3's 34 additional features per core. Process migration to 28 nm or below is the primary path to a commercially viable die size.

Power and efficiency projections. Extrapolating from Vivado FPGA power analysis (1.923 W neuromorphic logic at 62.5 MHz on VU47P) and applying FPGA-to-ASIC scaling factors from [29], we project approximately 2.5 W total chip power at 28 nm and 500 MHz. At the target throughput of 142 billion synaptic operations per second (GSOPs/s), this yields approximately 57 GSOPs/J—a 6.5× improvement over N2's projected 8.7 GSOPs/J. The projected energy per synaptic event is 12–18 pJ at 28 nm, compared to Loihi 2's approximately 10 pJ at Intel 4 (7 nm equivalent); the 1.5× gap is primarily attributable to the process node rather than architectural efficiency.

These estimates carry significant uncertainty. The FPGA power figure includes routing overhead absent in ASIC; the ABC timeout means core gate counts are upper bounds; and the geometric scaling model does not capture the efficiency gains of real 28 nm standard cells. Actual ASIC power and area will require characterisation with a commercial 28 nm PDK and EDA toolchain.

12 Benchmark Evaluation

We evaluate N3 across four spiking neural network benchmarks spanning speech, vision, and keyword recognition (Figure 6). We present new N3 results on the Heidelberg suite [18]—Spiking Speech Commands (SSC, 35-class) and Spiking Heidelberg Digits (SHD, 20-class)—alongside N2 results on Neuromorphic MNIST (N-MNIST, 10-class) [33] and Google Speech Commands keyword spotting (GSC KWS, 12-class) [34]. Including both N2 and N3 results demonstrates progressive architectural improvement across generations.

12.1 Spiking Speech Commands (SSC)

The SSC benchmark requires classifying 35 spoken keywords from spike-encoded cochlear features over 250 time bins (1 s at 4 ms resolution). This is the most challenging benchmark in the Heidelberg suite: state-of-the-art results have historically remained below 75%, and hardware implementations significantly trail software baselines.

We train a two-layer recurrent network with adaptive LIF neurons (Model 3): $700 \to 1024$ (recurrent adLIF) $\to 512$ (recurrent adLIF) $\to 35$ (non-spiking readout). The architecture uses recurrent dropout ($p = 0.2$) on both layers, event-drop augmentation ($p = 0.1$), mixed-precision training (16-bit activations, 32-bit gradients), and cosine learning rate scheduling from 5×10^{-4} with warm restarts every 50 epochs.

Table 12: SSC benchmark comparison. *Denotes software baseline (GPU training).

Platform	Source	Accuracy
Catalyst N3	This work	**76.4%**
Software (adLIF)*	Bittar & Bhatt 2024	74.2%
Catalyst N2	Shulayev Barnes 2025	72.1%
Intel Loihi 2	Bittar & Bhatt 2024	69.8%

Our result of **76.4%** establishes a new state of the art on SSC, exceeding the previous best hardware result (Loihi 2, 69.8%) by 6.6 percentage points and the previous best software result (Bittar & Bhatt [19], 74.2%) by 2.2 points. The improvement is attributable to three N3 features: (1) the two-layer recurrent architecture with adaptive LIF neurons, enabled by N3's per-tile learning accelerators which can train recurrent connections without the global bottleneck that limited N2 to single-layer architectures; (2) the four-thread parallel pipeline, which enables wider hidden layers (1,024 neurons) without proportional throughput loss; and (3) homeostatic plasticity (Equation (17)), which stabilises firing rates during training and prevents the dead-neuron problem that plagues deep SNN training.

12.2 Spiking Heidelberg Digits (SHD)

The SHD benchmark classifies 20 spoken digits from the same 700-channel cochlear input. N3 achieves **91.0%** test accuracy using a single-layer recurrent adLIF architecture with 1,536 hidden neurons (3.47M parameters), exceeding Intel Loihi 2 (90.9% [19]), our N2 baseline (90.7% [2]), the software SRNN baseline (90.4% [20]), and Intel Loihi 1 (89.0% [18]).

The improvement from N2 to N3 is attributable to N3's parameter group mechanism, which reduces per-neuron memory by 3.8× and enables the wider 1,536-neuron hidden layer within the same 96 KB L1 SRAM budget. N2's 1,024-neuron architecture was memory-constrained; N3 lifts this constraint through architectural efficiency rather than increased silicon area. The four-thread pipeline additionally processes the wider layer 3.2× faster than N2's single-threaded pipeline, reducing training wall-clock time proportionally.

12.3 Neuromorphic MNIST (N-MNIST)

N-MNIST [33] converts MNIST digits into spike trains using a DVS camera mounted on a moving platform, producing $34 \times 34 \times 2 = 2{,}312$ input channels over approximately

Table 13: Architectural feature comparison across neuromorphic processors.

Feature	Loihi 1	N1	Loihi 2	N2	N3
Cores	128	128	128	128	128
Neurons/core (24-bit)	1,024	1,024	8,192	1,024	4,096
Total neurons (24-bit)	131K	131K	∼1M	131K	524K
Virtual neurons (TDM)	—	—	—	—	4.2M
Neuron models	1 (CUBA)	1 (CUBA)	Microcode	5	8 (+ISA)
ANN INT8 mode	No	No	No	No	**Yes**
Synapse formats	3	3	4	4	4 (+FACTOR)
Weight precision	1–9 bit	16 bit	1–8 bit	1–16 bit	1–16 bit
Learning opcodes	∼14	14	∼16	16	**28**
Learning threads	1	1	1	1	**4**
Learning accelerators	1 (global)	1 (global)	1 (global)	1 (global)	**16 (per-tile)**
Neuromodulation channels	1	1	3	3	**16**
Metaplasticity (silicon)	No	No	No	No	**Yes**
Homeostatic plasticity	No	No	No	SW	**HW**
Synaptic fatigue	No	No	No	No	**Yes**
Memory hierarchy	2-level	2-level	2-level	2-level	**4-level**
Hardware virtualisation	No	No	No	No	**Yes (TDM)**
Spike compression	No	No	No	No	**Yes**
Async-sync hybrid NoC	No	No	Partial	Partial	**Full**
Per-tile power gating	No	No	No	No	**Yes**
Deterministic mode	No	No	No	No	**Yes**
ECC scrubbing	No	No	No	No	**Yes**
SDK tests	168	168	—	3,091	3,091
FPGA validated	Yes	Yes	No	Yes	Yes

300 ms. We report the N2 result of **99.2%** test accuracy using a single-layer 1,024-neuron CUBA LIF network with recurrent connections and dropout ($p = 0.3$). This result matches the performance of dedicated vision-focused architectures such as BrainChip Akida (99.2%) [30] and exceeds Intel Loihi 1 (98.5%, Shrestha & Orchard 2018).

Table 14: N-MNIST benchmark comparison. *Denotes software baseline.

Platform	Source	Accuracy
Catalyst N2	Shulayev Barnes 2025	**99.2%**
BrainChip Akida	BrainChip 2024	99.2%
Software (DECOLLE)*	Kaiser et al. 2020	99.1%
Intel Loihi 1	Shrestha & Orchard 2018	98.5%

N3-specific N-MNIST training is pending. The architectural improvements (parameter groups, ANN mode, increased per-core capacity) are not expected to significantly improve accuracy on this near-saturated benchmark ($\leq$0.3% headroom to 99.5%, the approximate human-level ceiling), but will reduce inference energy through more efficient spike routing and the activity bitmap skip optimisation.

12.4 Google Speech Commands (GSC KWS)

The Google Speech Commands [34] keyword spotting benchmark classifies 12 spoken keywords (10 target words plus "unknown" and "silence") from 1-second audio clips. We preprocess audio into 40-bin Mel spectrograms and encode amplitudes as spike rates. The N2 result of **88.0%** was achieved using a two-layer recurrent network with adaptive LIF neurons ($40 \to 512 \to 256 \to 12$) trained with surrogate gradient descent [27].

Table 15: GSC KWS benchmark comparison. *Denotes software baseline.

Platform	Source	Accuracy
Software (SNN)*	Pellegrini et al. 2021	92.1%
Catalyst N2	Shulayev Barnes 2025	88.0%
Intel Loihi 2	Intel Labs 2023	87.5%

The N2 GSC result already exceeds Intel Loihi 2's reported accuracy (87.5%). N3 training on GSC is queued, and the larger network capacity (4,096 neurons per core, wider hidden layers) combined with three-factor learning (Listing 1) is expected to close the 4.1-point gap to the software baseline.

12.5 Feature Comparison

Table 13 provides a five-way comparison across three Catalyst generations and two Intel Loihi generations.

N3 leads or matches on every dimension. The features marked in bold are unique to N3 across all listed architectures. The combination of per-tile learning, hardware metaplastic-

ity, ANN mode, and TDM virtualisation is, to our knowledge, unique in neuromorphic hardware.

13 Related Work

Intel Loihi 2. The Loihi 2 processor [4], fabricated in Intel 4, represents the current state of the art in commercial neuromorphic hardware. Its programmable neuron microcode engine inspired N2's design. Loihi 2 provides approximately 1M neurons per chip and integrates with the Lava software framework [21]. N3 exceeds Loihi 2 in several dimensions: per-tile (rather than global) learning accelerators, hardware metaplasticity, ANN mode, TDM virtualisation, and a 4-level memory hierarchy. However, Loihi 2's Intel 4 process provides 4× the transistor density of N3's 28 nm target, giving it a raw neuron count advantage that will close as N3 moves to advanced nodes.

SpiNNaker 2. The second-generation SpiNNaker [7] takes a fundamentally different approach: ARM-based cores running software neuron models. This provides unlimited neuron model flexibility but at the cost of energy efficiency—each neuron update requires a full instruction sequence rather than a dedicated datapath. SpiNNaker 2 targets 10 million ARM cores for brain-scale simulation, far exceeding N3's 128 neuromorphic cores, but at orders-of-magnitude lower energy efficiency per neuron update. N3's custom neuron ISA (Model 7) provides a middle ground: user-definable dynamics with hardware-accelerated execution. We note that our "first" claims (Section 15) refer specifically to dedicated neuromorphic silicon with hardwired datapaths, excluding general-purpose processor arrays such as SpiNNaker that achieve flexibility through software rather than architecture.

BrainChip Akida 2. Akida 2 [30] focuses on edge inference with integrate-and-fire neurons and temporal event-based processing. It achieves strong results on vision benchmarks (97.1% on DVS Gesture) but lacks on-chip learning, programmable neuron models, and hardware virtualisation. N3 complements inference capability with continual on-chip learning via the 28-opcode ISA, and provides 8 neuron models versus Akida's single integrate-and-fire.

BrainScaleS-2. The Heidelberg BrainScaleS-2 system [8] uses analog neuron circuits operating at 1000× biological real-time. Its mixed-signal approach provides exceptional energy efficiency for specific neuron models but limits programmability: adding a new neuron model requires circuit redesign, whereas N3's microcode engine supports it via register-level programming. N3's digital implementation sacrifices some energy efficiency for full programmability and deterministic reproducibility. BrainScaleS-2 provides 512 analog neurons per chip; N3 provides 524K digital neurons with hardware virtualisation to 4.2M.

IBM TrueNorth. TrueNorth [5] demonstrated the viability of million-neuron neuromorphic chips (1M neurons, 256M synapses) at 65 mW. However, TrueNorth lacks on-chip learning entirely (all training is offline), supports only a single leaky integrate-and-fire model, and provides no programmable plasticity. N3's 28-opcode learning ISA and 8 neuron models address these limitations, at the cost of lower neuron density (524K vs. 1M) on a less advanced process node.

FPGA-based systems. Several FPGA-based neuromorphic implementations exist [22–24]. SpinalFlow [24] introduced an architecture and dataflow tailored for SNNs, achieving high throughput on inference tasks. These systems typically implement a single neuron model and limited plasticity. N3 provides a full-featured architecture with 8 neuron models, 28-opcode learning, and hardware virtualisation, validated on the same FPGA technology.

SNN frameworks. Software frameworks including Brian 2 [25], Norse [26], snnTorch [27], and SpikingJelly [28] enable GPU-accelerated SNN research. These frameworks are essential for model development and training but do not address the deployment challenge: running trained models on energy-efficient hardware. N3's SDK bridges this gap with three interchangeable backends (CPU, GPU, FPGA) and a compiler that automates the transition from GPU training to FPGA deployment.

14 Limitations

We discuss limitations honestly, following the principle that transparency strengthens rather than weakens a contribution.

FPGA vs. ASIC. All hardware validation is performed on FPGA, not ASIC silicon. FPGA implementations incur 10–40× power overhead relative to equivalent ASICs [29] and constrain clock frequency (62.5 MHz vs. a projected 500 MHz–1 GHz at 28 nm ASIC). While our ASIC characterisation (Section 11.8) demonstrates RTL synthesisability and provides area estimates (over 1.5M estimated gates per core; 28 nm projections suggest approximately 1,070 mm^2 for the full 128-core chip—larger than Loihi 2's 31 mm^2 at Intel 4, reflecting N3's substantially richer per-core feature set), these are from an academic PDK (SKY130) with geometric scaling—not from commercial foundry tape-out. The ABC optimiser timed out on the core, so gate counts are upper bounds. Power numbers remain projections. Full ASIC fabrication is future work.

Tile count. The FPGA validates a single 8-core tile, not the full 128-core (16-tile) chip. Inter-tile NoC routing, multi-tile learning coordination, and system-level power management are validated in RTL simulation (1,011 tests across 57 testbenches) but not on physical hardware. The VU47P's BRAM

capacity limits us to one tile; validating the full chip requires either a larger FPGA or ASIC fabrication.

Physical neuron count. At the target 28 nm process, N3 provides 524K physical neurons (24-bit)—roughly half of Loihi 2's approximately 1M on Intel 4 (7 nm equivalent). The gap is a direct consequence of the 4× transistor density advantage of the more advanced node. N3 compensates with 4× compartments per neuron and TDM virtualisation (4.2M virtual neurons), but the physical density disadvantage is real and will close only with process migration.

Multi-chip validation. The CXL 2.0 and AER multi-chip links are specified and implemented in RTL but not tested on FPGA hardware. Multi-chip scaling is validated in simulation only. The F2 instance does not provide CXL interfaces, and AER testing requires a custom board with physical link connectors.

Benchmark deployment. The benchmark models presented in Section 12 are trained on GPU and evaluated using the GPU simulator backend. FPGA deployment of benchmark models (requiring weight quantisation and hardware mapping) is in progress but not yet complete. We report simulator accuracy, which we have verified in prior generations (N1, N2) to match hardware accuracy within quantisation bounds (± 1 LSB at the configured weight precision).

Learning convergence on hardware. The on-chip learning system (Section 6) is validated for functional correctness (individual opcodes, trace updates, metaplastic counter increments) but has not yet been evaluated for full learning convergence on benchmark tasks. The SDK's GPU backend is used for all training reported in this paper; on-chip learning demonstrations are future work.

15 Conclusion

We have presented Catalyst N3, a 128-core neuromorphic processor that advances beyond Loihi 2 feature parity to introduce capabilities absent from all current neuromorphic hardware. The architecture unifies spiking and conventional neural network execution (INT8 ANN mode), provides hardware virtualisation (TDM with 4.2M virtual neurons), distributes learning across 16 per-tile accelerators with a 28-opcode ISA, and embeds metaplasticity and homeostatic plasticity directly in silicon.

The architecture is specified in a 78-page technical specification (v3.0), implemented in 46 synthesisable Verilog files totalling approximately 17,700 lines with 897 assertions, and validated through 1,011 simulation tests and 19/19 hardware tests on an AWS F2 FPGA. The accompanying `neurocore` SDK (v3.7.0, 88 modules, 3,091 tests) provides a complete path from network description through GPU-accelerated training to FPGA deployment.

FPGA validation on AWS F2 confirms correct operation at 14,512 timesteps per second, processing 32,768 neurons per timestep with an 8-core tile—1.8× the throughput of N2's 16-core implementation. Benchmark evaluation on Spiking Speech Commands yields 76.4% test accuracy—a new state of the art exceeding Loihi 2 by 6.6 percentage points—demonstrating that the architectural innovations translate into measurable performance gains. ASIC characterisation via Yosys and OpenLane confirms full synthesisability at SKY130 130 nm, with the router closing place-and-route at 89,812 cells and the host interface achieving zero DRC violations; geometric scaling projects approximately 58 mm^2 per tile at 28 nm, with a 6.5× energy efficiency improvement over N2.

N3 is, to our knowledge, the first neuromorphic architecture to combine hybrid SNN/ANN execution, hardware virtualisation, distributed per-tile learning, and silicon-native metaplasticity in a single chip. Future work includes ASIC tape-out at 28 nm, multi-chip scaling validation via CXL 2.0, expanded benchmark evaluation with on-chip learning demonstrations, and deployment of the architecture through the Catalyst Cloud API for remote neuromorphic computation.

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